Notice of Allowability	Application No.	Applicant(s)	
	10/825,189	ARIMILLI ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 7/13/07*.

2. ☒ The allowed claim(s) is/are *2-5,8,9,11-15,17 and 19-22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

In view of Applicant's amendments, the objections to specification have been withdrawn.

In view of Applicant's amendments, the 112, second paragraph rejections to claims 2-7 and 17-22 have been withdrawn.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Eustace P. Isidore, Reg. No. 56,104, on September 24, 2007 and September 27, 2007.

The application has been amended as follows:

- Amended **claim 2** reads as follows:

2. In a data processing system having multiple processors each having a processor core, store queue (STQ) mechanism, read claim (RC) mechanism, and associated

processor cache, a method for facilitating cache line updates responsive to processor-issued store operations, said method comprising:

determining when a store queue entry selected for dispatch by an RC machine provides an update to an entire cache line by:

tracking processor issued store operations gathered to said store queue entry via byte enable bits, wherein each storage granule of multiple storage granules within said store queue entry is provided a corresponding byte enable bit that is set to a logical high value when the storage granule is updated by a store operation, wherein the byte enable bit retains a logical low value when no update occurs to the corresponding storage granule, wherein each of multiple byte enable bits corresponding to the multiple storage granules are set to the logical high value when all the storage granules within the entry have been updated;

logically ANDing each of the multiple byte enable bits of the store queue entry to determine when all storage granules of said store queue entry have been updated; and

providing a full signal to a STQ controller when said logically ANDing step results in a logical high value, which indicates that all storage granules of said entry have been updated; and

completing said update to said entire cache line with address-only operations, wherein no data tenure is requested when an entire cache line is being overwritten, wherein said completing includes:

receiving at said RC mechanism an entry select identifying the entry for dispatch;

receiving at said RC mechanism a signal indicating that the entry is full;

assigning the cache line update operation to an RC machine of said RC mechanism;

providing an indication to the RC machine that the entire cache line is being updated; and

responsive to a receipt by said RC machine of the full signal indicating that the entry being dispatched is full, activating a cache update mechanism that enables the completion of the cache line update without requiring a copy of the cache line or current data within the cache line, wherein cache line updates from entries that are not full are completed with a current copy of the cache line within the cache and write permission to the cache line.

- **Claim 6** has been canceled

- **Claim 7** has been canceled

- Amended **claim 9** reads as follows:

9. A processor chip for utilization within a data processing system having a memory hierarchy, said processor chip comprising:

a processor core;

a store queue having multiple entries, each entry including registers for storing address and data of store operations issued by the processor core and multiple byte-enable bits, one for each smallest storage granule of data that may be stored by a store operation, wherein each byte enable bit corresponds to one of the smallest storage granule among the multiple storage granules within the entry and each bye enable bit is set to a logical high value when the storage granule is updated by a store operation, wherein the byte enable bit retains a logical low value when no update occurs to the corresponding storage granule, wherein each of multiple byte enable bits corresponding to the multiple storage granules are set to the logical high value when all the storage granules within the entry have been updated;

a store queue (STQ) controller that monitors and controls said store queue;

arbitration logic associated with said STQ controller that selects an entry from among multiple eligible entries available for dispatch to be stored in a lower level cache; and

an read claim (RC) mechanism that perform updates to cache lines within said lower level cache utilizing data from the entry selected for dispatch; and

first logic for determining when all storage granules within a store queue entry have received data from said processor core before said entry is selected for dispatch, wherein said first logic comprises AND logic associated with each of said entries that receives as input a value of each of said multiple byte-enable bits and provides a single AND output that indicates when all of said multiple byte-enable bits for the entry are set, indicating a full entry; and

second logic within an RC machine of said RC mechanism assigned to update a target cache line with data of said entry for completing said update of the target cache line without initiating a data tenure on the system bus, wherein said update is completed regardless of whether said cache line is present in said lower level cache or said cache line data is stale, wherein said second logic includes logic for:

receiving at said RC mechanism an entry select identifying the entry for dispatch;

receiving at said RC mechanism a signal indicating that the entry is full;

assigning the cache line update operation to the RC machine of said RC mechanism;

providing an indication to the RC machine that the entire cache line is being updated; and

responsive to a receipt by said RC machine of the full signal indicating that the entry being dispatched is full, activating a cache update mechanism that enables the completion of the cache line update without requiring a copy of the cache line or current data within the cache line, wherein cache line updates from entries that are not full are completed with a current copy of the cache line within the cache and write permission to the cache line.

- Amended **claim 17** reads as follows:

17. A data processing system comprising:

a processor chip having a processor core, store queue (STQ) mechanism, read claim (RC) mechanism, and associated processor cache;

wherein:

said store queue mechanism includes a store queue with a plurality of entries, each entry having at least a data and address register and multiple byte-enable bits, wherein each byte enable bit corresponds to one of the smallest storage granule among the multiple storage granules within the entry and each bye enable bit is set to a logical high value when the storage granule is updated by a store operation, wherein the byte enable bit retains a logical low value when no update occurs to the corresponding storage granule, wherein each of multiple byte enable bits corresponding to the multiple storage granules are set to the logical high value when all the storage granules within the entry have been updated; and

said processor chip further includes first logic for determining when a store queue entry selected for dispatch by the RC mechanism provides a complete update to a target cache line of the processor cache, wherein said first logic for completing said determining comprises AND logic associated with each of said entries that receives as input a value of each of said multiple byte-enable bits and provides a single AND output that indicates when all said multiple byte-enable bits of the entry are set, indicating a full entry; and

said RC mechanism assigned to complete said update includes second logic for completing said update to said target cache line with address-only operations, wherein no data tenure is requested when the target entire cache line is being completely updated;

a memory hierarchy coupled to said processor chip and providing coherent memory operation;

means for completing the update to the entire cache line of the processor cache with the data from the processor-issued stores via a single address-only system bus tenure, with no data tenure, wherein when all storage granules of said cache line are being updated by a single RC machine tenure, the update is completed without initiating a data tenure on the system bus, regardless of whether the cache line being updated is present in the processor cache or whether the cache line is present but contains stale data, wherein said means for completing includes means for:

receiving at said RC mechanism an entry select identifying the entry for dispatch;

receiving at said RC mechanism a signal indicating that the entry is full;

assigning the cache line update operation to an RC machine of said RC mechanism;

providing an indication to the RC machine that the entire cache line is being updated; and

responsive to a receipt by said RC machine of the full signal indicating that the entry being dispatched is full, activating a cache update mechanism that enables the completion of the cache line update without requiring a copy of the cache line or current data within the cache line, wherein cache line updates from entries that are not full are completed with a current copy of the cache line within the cache and write permission to the cache line.

Allowable Subject Matter

Claims 2-5, 8, 9, 11-15, 17, and 19-22 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination including the limitations of:

(**Claims 2, 9, and 17**) "...receiving at said RC mechanism an entry select identifying the entry for dispatch; receiving at said RC mechanism a signal indicating that the entry is full; assigning the cache line update operation to an RC machine of said RC mechanism; providing an indication to the RC machine that the entire cache line is being updated; and responsive to a receipt by said RC machine of the full signal indicating that the entry being dispatched is full, activating a cache update mechanism that enables the completion of the cache line update without requiring a copy of the cache line or current data within the cache line, wherein cache line updates from entries that are not full are completed with a current copy of the cache line within the cache and write permission to the cache line."

As dependent claims **3-5, 8, 11-15, and 19-22** depend from an allowable base claim, they are at least allowable for the same reasons as noted above.

Any comments considered necessary by Applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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September 27, 2007

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